CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A transmitter, comprising:

(a) a convolutional encoder capable of receiving a plurality of bits on tones and capable of outputting a convolutionally encoded plurality of bits; and

(b) a synchronized dual skipping switch capable of passing the plurality of bits on tones to the convolutional encoder in a non-sequential order and capable of outputting the convolutionally encoded plurality of bits in the non-sequential order.

2. The transmitter of claim 1, further including:

(c) a mapper capable of mapping the convolutionally encoded plurality of bits to two constellation points in an encoder constellation table.

3. The transmitter of claim 1, wherein the non-sequential order skips 3 tones.

4. The transmitter of claim 1, wherein the non-sequential order skips 4 tones.

5. The transmitter of claim 1, wherein the non-sequential order is variable.

6. The transmitter of claim 5, wherein the non-sequential order is dynamically determined by a receiver.

7. The transmitter of claim 1, wherein the non-sequential order skips $1/8^{th}$ of the tones .

8. The transmitter of claim 1, wherein the plurality of bits on tones are DMT symbols.

9. The transmitter of claim 1, further including:

(c) a constellation buffer, wherein the constellation buffer receives the covolutionally encoded plurality of bits from the synchronized dual skipping switch.

10. The transmitter of claim 1, wherein the synchronized dual skipping switch passes the plurality of bits on tones from a bit extractor buffer to the convolutional encoder and outputs the convolutionally encoded plurality of bits to a constellation buffer.

11. The transmitter of claim 1, wherein the convolutional encoder is forced to a zero state prior to the start of a data frame.

12. A transmitting system, comprising:

(a) means for convolutionally encoding a plurality of bits on tones;

(b) means for buffering the convolutionally encoded plurality of bits; and

(c) means for non-sequentially switching the plurality of bits on tones to the means for convolutionally encoding, in sync with switching the convolutionally encoded plurality of bits from the means for convolutionally encoding to the means for buffering.

13. The transmitting system of claim 12, further comprising:

(d) means for mapping the convolutionally encoded plurality of bits before switching the convolutionally encoded plurality of bits from the means for convolutionally encoding to the means for buffering.

14. The transmitting system of claim 12, wherein the means for non-sequential switching is a variable means for non-sequential switching.

15. The transmitting system of claim 14, wherein the means for non-sequential switching is dynamically controlled by a receiver.

16. The transmitting system of claim 12, wherein the plurality of bits on tones are DMT symbols.

17. A method for transmitting data, comprising the steps of:

(a) receiving a first plurality of bits on a first tone from a bit extractor buffer through a synchronized dual skipping switch;

(b) receiving a second plurality of bits on a second tone from the bit extractor through the synchronized dual skipping switch, wherein the second tone is not adjacent to the first tone;

(c) convolutionally encoding the first and second pluralities of bits; and

(d) outputting the convolutionally encoded first and second pluralities of bits through the synchronized dual skipping switch.

18. The method of claim 17, further comprising:

(e) mapping the convolutionally encoded first and second pluralities of bits.

19. The method of claim 18, further comprising:

(f) buffering the mapped and convolutionally encoded first and second pluralities of bits.

20. The method of claim 17, wherein the first and second tones are separated by a variable number of tones.

21. The method of claim 20, wherein the variable number of tones is determined by a receiver.

22. The method of claim 17, wherein the first and second pluralities of bits are DMT symbols.

23. A computer readable medium, comprising:

(a) logic for convolutionally encoding a plurality of bits on tones;

(b) logic for buffering the convolutionally encoded plurality of bits; and

(c) logic for non-sequentially connecting the plurality of bits on tones to the logic for convolutionally encoding, in sync with connecting the convolutionally encoded plurality of bits from the logic for convolutionally encoding to the logic for buffering.

24. The computer readable medium, further comprising:

(d) logic for mapping the convolutionally encoded plurality of bits before connecting the convolutionally encoded plurality of bits from the logic for convolutionally encoding to the logic for buffering.

25. The computer readable medium, wherein the logic for non-sequential connecting is logic for variably non-sequentially connecting.

26. The computer readable medium of claim 25, wherein the logic for non-sequentially connecting is dynamically controlled by a receiver.

27. The computer readable medium of claim 23, wherein the plurality of bits on tones are DMT symbols.

28. A transmitter, comprising:

(a) a limited plurality of inputs, the inputs being two bits of a binary word derived from a DMT symbol;

(b) a limited plurality of convolutional encoders capable of producing an output, the output based on unit time delays and logic gates, and the limit on the plurality convolutional encoders being equal to the limit on the plurality of inputs; and

(c) a synchronized dual switch, wherein the synchronized dual switch is designed to perform the following:

(1) connect the first of the limited plurality of inputs to the first of the limited plurality of convolutional encoders and connect the output from the connected convolutional encoder to a coset mapper;

(2) connect the second of the limited plurality of inputs to the second of the limited plurality of convolutional encoders and connect the output from the connected convolutional encoder to the coset mapper; and

(3) continue connecting successive inputs to the successive convolutional encoders and connecting the output from the connected convolutional encoder to the coset mapper until the limit is reached.

29. The transmitter of claim 28, wherein the limit is variable.

30. The transmitter of claim 29, wherein the variability is dynamically controlled by a receiver.

31. The transmitter of claim 28, wherein the plurality of convolutional encoders are set to zero prior to the start of a data frame.

32. A transmitter, comprising:

(a) an input, the input being two bits from a binary word;

(b) a plurality of logic gates;

(c) a plurality of variable unit time delays, the variable unit time delays storing values based on previous inputs; and

(d) an output, wherein the output includes the input and a third bit based on the inputs, the stored values, and the logic gates.

33. The transmitter of claim 32, wherein the variability of the variable unit time delays is dynamically controlled by a receiver.

34. The transmitter of claim 32, wherein the variable unit time delays are set to zero prior to the start of each of a data frame.

35. A receiver, comprising:

(a) a convolutional decoder capable of receiving a plurality of bits on tones and capable of outputting a convolutionally decoded plurality of bits; and

(b) a synchronized dual skipping switch capable of passing the plurality of bits on tones to the convolutional decoder in a non-sequential order and capable of outputting the convolutionally decoded plurality of bits in the non-sequential order.

36. The receiver of claim 35, wherein the non-sequential order is the same non-sequential order in which the plurality of bits on tones were convolutionally encoded.

37. The receiver of claim 35, further including:

(c) a demapper capable of demapping the plurality of bits on tones.

38. The receiver of claim 35, wherein the non-sequential order is variable.

39. The receiver of claim 35, wherein the plurality of bits on tones are DMT symbols.

40. The receiver of claim 35, further including:

(c) a bit buffer, wherein the bit buffer receives the convolutionally decoded plurality of bits from the synchronized dual skipping switch.

41. The receiver of claim 35, wherein the synchronized dual skipping switch passes the plurality of bits on tones from a DFT to the convolutional decoder and outputs the convolutionally decoded plurality of bits to a bit buffer.

42. A method for receiving data, comprising the steps of:

(a) receiving a first plurality of bits on a first tone through a synchronized dual skipping switch;

(b) receiving a second plurality of bits on a second tone through the synchronized dual skipping switch, wherein the second tone is not adjacent to the first tone;

(c) convolutionally decoding the first and second plurality of bits; and

(d) outputting the convolutionally decoded first and second pluralities of bits through the synchronized dual skipping switch.

43. The method of claim 42, further including:

(e) demapping the first and second pluralities of bits on tones.

44. The method of claim 42, wherein the first and second tones are separated by a variable number of tones.

45. The method of claim 42, wherein the first and second tones are separated by the same number of tones as in the transmitter that sent the first and second pluralities of bits on tones.

46. The method of claim 42, wherein the first and second pluralities of bits on tones are DMT symbols.

47. A receiver, comprising:

(a) a limited plurality of inputs, the inputs being two bits of a binary word derived from a convolutionally encoded DMT symbol;

(b) a limited plurality of convolutional decoders capable of producing an output, the output based on unit time delays and logic gates, and the limit on the plurality of convolutional decoders being equal to the limit on the plurality of inputs; and

(c) a synchronized dual switch, wherein the synchronized dual switch is designed to perform the following:

(1) connect the first of the limited plurality of inputs to the first of the limited plurality of convolutional decoders and connect the output from the connected convolutional decoder to a bit orderer;

(2) connect the second of the limited plurality of inputs to the second of the limited plurality of convolutional decoders and connect the output from the connected convolutional decoder to the bit orderer; and

(3) continue connecting successive inputs to the successive convolutional decoders and connecting the output from the connected convolutional decoder to the bit orderer until the limit is reached.

48. The receiver of claim 47, wherein the limit is variable.